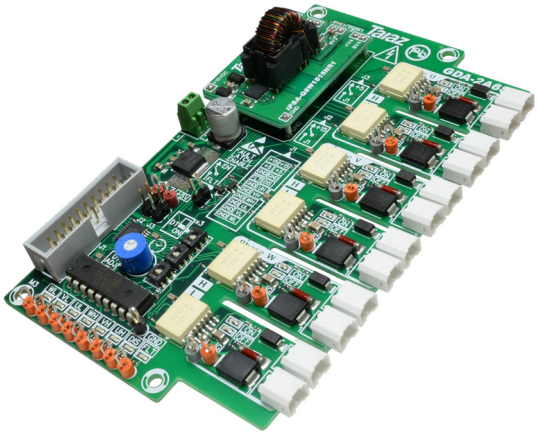
GDA-2A6S1

Isolated 6SW 3Phase 2A Smart Gate Drive Module



Features

- Best Cost to Performance Ratio in the Market.
- Suitable for 1200V IGBTs and Power MOSFETs up-to 120A.
- 2A Peak Gate Drive Current.
- 3000 V_{RMS} Input to Output Isolation.
- Short-Circuit Protection Through Desaturation Detection.
- Active Miller Protection.
- Output UVLO Protection.
- Output Clamping Protection.
- Isolated Fault Feedback.
- Soft IGBT Turnoff in Case of Fault.
- Configurable Fault Latch Shutdown.
- Configurable PWM/Dual Inputs.
- Configurable Dead-Time.
- 50KV/us Minimum Common Mode Rejection (CMR).
- Very Low Propagation Delay of 250ns (Maximum) for High Frequency Operation.
- Input & Output Indication LEDs for Visual Feedback.
- Input & Output Test points for easy testing.
- Built-in 5V Regulator for Powering up External Control Circuitry.

Applications

- 6 Switch Isolated IGBT/MOSFET Gate Drive
- AC & Brushless DC Motor Drives
- 3 Phase PFC Rectifiers
- R&D Inverters

Compliance

- ROHS

Description

The GDA-2A6S1 is high performance fully isolated IGBT/MOSFET gate drive module for 3Phase 6Switch configuration. It is specially designed for fastest inverter prototyping in research and educational environments. The drive use's Avago ACPL-332J smart and high performance gate driver IC, and feature's dead time generation logic, fault latch logic, input and output indication LEDs, test points and built in 5V regulator which could be used to power up external control circuitry.

But the most notable feature of this module is that it detects short circuit condition using desaturation detection and can safely turn off the switch and give the controller an isolated fault feedback signal. The user can also enable fault latch circuitry which automatically shuts down the module and does not resume operation till complete power reset.

This product can be ordered with different input and output connectors, making it suitable as a plugin module, PCB mounted module or free hanging module.

Revision History Table

Version	Release Date	Changes
0.1	16/08/2015	First Version Released

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Table of Contents

Ratings & Characteristics

*All ratings are given at Vs=15V and 25°C ambient temperature unless otherwise specified.

Absolute Maximum Ratings	Test Conditions/ Note	Value	Unit
Supply Voltage (V_S)		18	V
Input Signal Voltage HIGH		5.5	V
Input Signal Voltage LOW		0	V
Output Peak Current ($I_{out(PEAK)}$)	Using Rg<10Ω	2	A
Output Average Current ($I_{out(AVG)}$)	Per Channel	40	mA
Output Power (P_{out})	Per Channel	0.6	W
Active Miller Clamp Current		1.7	A
Maximum Working Insulation Voltage	Vpeak	707	V
Input to Output Isolation	AC RMS	3000	V
J1 5V Output Current (I_{OUT5V})	Supply for external circuit	180	mA
Operating Temperature	I_{OUT5V} = 0	-25 to +70	°C
Storage Temperature		-25 to +85	°C

Recommended Operating Conditions	Test Conditions/ Note	Minimum	Typical	Max	Unit
Supply Voltage (Vs)		13	15	17	V
Supply Current			100	300	mA
Operating temperature	I_{OUT5V} = 0	-10	-	70	°C
Input Signal Voltage On/Off	3.3V control signals possible		5/0		V

Ratings & Characteristics (Continued)

*All ratings are given at Vs=15V and 25°C ambient temperature unless otherwise specified.

Characteristics	Test Conditions/ Note	Minimum	Typical	Max	Unit
Logic High Input Threshold		2.0	-	-	V
Logic Low Input Threshold		-	-	0.8	V
Output Voltage HIGH (VoH)	V_S = 15V, 20mA $I_{out(AVG)}$	11.16	12.06	12.23	V
Output Voltage LOW (VoL)	V_S = 15V	-	0.17	0.5	V
Output UVLO Threshold	UVLO + UVLO -	10.5 9.2	11.6 10.3	12.5 11.1	V
Output Clamp Threshold	Of Bi-directional TVS @ 1mA	16.7	-	18.5	V
Fault Output Voltage	Active LOW	-	-	0.8	V
Input Impedance	All inputs have 10 kΩ pull-down resistors	-	10	-	kΩ
Internal Gate to Emitter Resistance		-	6.2	-	kΩ
Duty Cycle Range		0	-	100	%
Configurable Dead-time	Using DT-ADJ	0.58	-	9.28	us
Propagation Delay	R_g=10Ω, C_g=10nF, f=10kHz, Duty Cycle = 50%	100	180	250	ns
Pulse Width Distortion	R_g=10Ω, C_g=10nF, f=10kHz, Duty Cycle = 50%	-100	20	100	ns
Output Rise and Fall Time	R_g=10Ω, C_g=10nF, f=10kHz, Duty Cycle = 50%	-	50	-	ns
DESAT Threshold		6	6.5	7.5	V
DESAT Sense to 90%VO Delay ($t_{DESAT(90\%)}$)		-	0.15	0.5	us
DESAT Sense to 10% VO Delay ($t_{DESAT(10\%)}$)		-	2	3	us
DESAT Sense to Low Level FAULT Signal Delay ($t_{DESAT(FAULT)}$)		-	0.25	0.5	us
DESAT Input Mute ($t_{DESAT(MUTE)}$)		5	-	-	us
RESET to High Level FAULT Signal Delay ($t_{RESET(FAULT)}$)		0.3	1	2	us
DESAT Blanking Time (t_{BLANK})		-	2.7	-	Us
Common Mode Rejection (CMR)	At V_{CM}=1500V	50	60	-	kV/us
Weight	PX/TP Option	-	59	-	g
Dimensions (Bare)	Width x Length x Depth		74 x 127 x 29.32		mm

Block Diagram

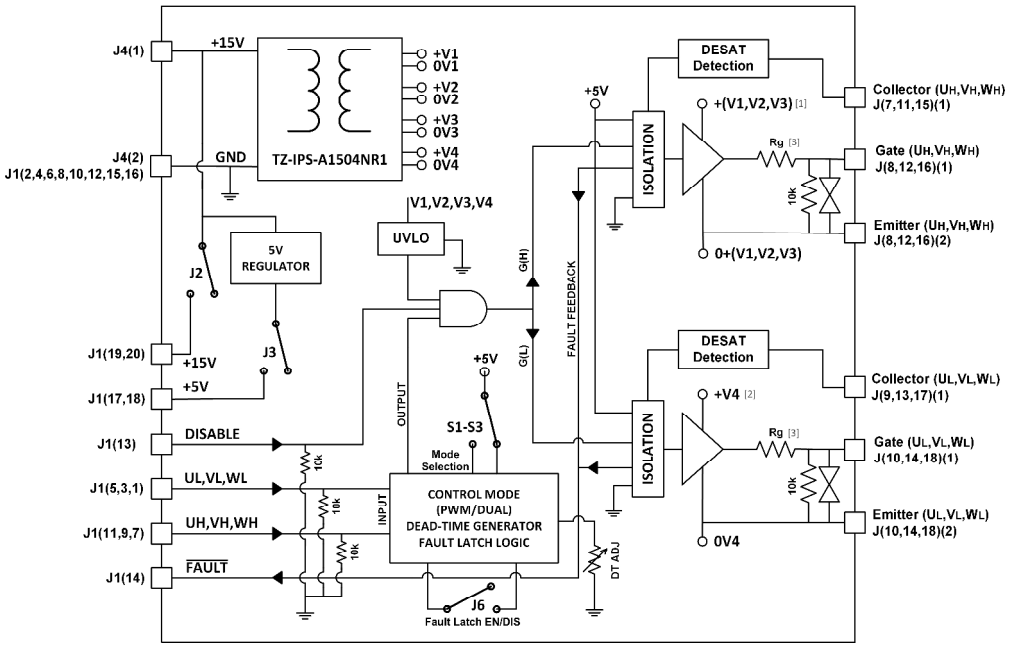
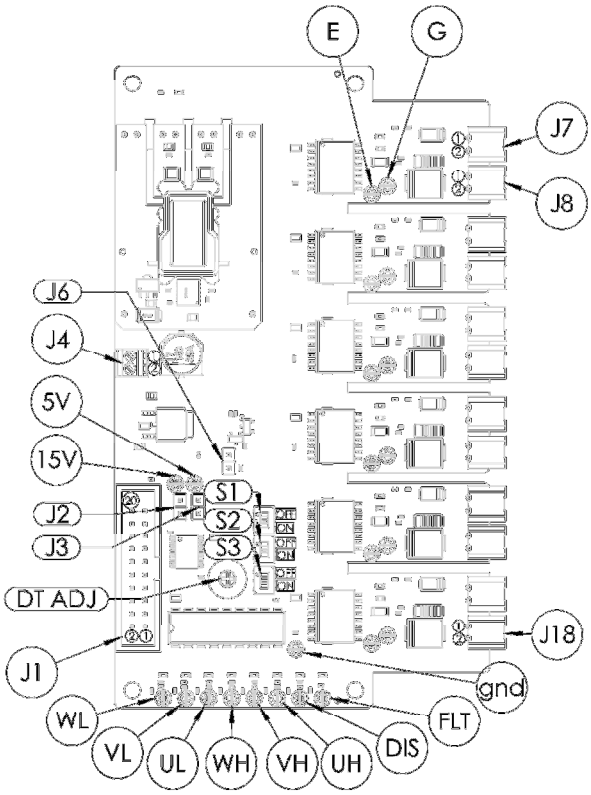


Figure 1: Block Diagram

Notes:

1) All three upper drivers are powered by isolated (floating) voltage sources (V1, V2 and V3).
2) All three lower drivers are powered by same voltage source (V4), since all lower switches share the emitter terminal.
3) The default gate resistor is 10Ω and user can control the gate turn on and off by changing Rg to lower value for faster switching, or higher value to minimize ringing. However, the minimum value to be used should be greater than or equal to IGBT/MOSFET datasheet recommended value for reliable operation.
4) In case of PWM mode, control signals will be generated from UH, VH & WH. User don't have to supply the UL, VL & WL signals.

Pin Description



Name	Connector (Pin No.)	Description
UH, VH, WH	J1 (11,9,7)	Non-inverting logic input terminal for HIGH side gate.
UL, VL, WL	J1 (5,3,1)	Non-inverting logic input terminal for LOW side gate. (Dual mode only)
GND	J4(2), J1 (2,4,6,8,10,12,15,16)	Ground
+15V	J4(1), J1 (19,20)	+15V supply voltage (V_S) for the module. It can be supplied either from J4 or J1 (if J2 is connected).
+5V	J1 (17,18)	+5V supply output from the module to power up the external circuit. Enabled by connecting J3.
DISABLE	J1 (13)	Input disable signal, active high will drive all outputs to LOW.
$\overline{\text{FLT}}$	J1 (14)	Fault feedback output, active low. When a fault condition occurs, this pin will move into low state.
Collector	J(7,9,11,13,15,17)(1)	Output to IGBT/MOSFET collector terminal (must be connected).
NC	J(7,9,11,13,15,17)(2)	This pin is not connected.
Gate	J(8,10,12,14,16,18)(1)	Output to IGBT/MOSFET gate terminal.
Emitter	J(8,10,12,14,16,18)(2)	Output to IGBT/MOSFET emitter terminal.
FAULT LATCH DISABLE	J6	By default this is not connected and the fault latch is enabled. This results in circuit operation to be disabled (until power reset) in case of fault condition. When connected, fault latch will be disabled, the circuit will resume operation after blanking time (2.7us).
15V to J1	J2	If user wish to supply +15V from J1 then J2 jumper must be connected.
5V to J1	J3	If user wish to power up the external control circuitry from gate drive module then +5V can be supplied to J1 by connecting J3 jumper.
Dead-Time Adjust	DT-ADJ	Duration of Dead-time can be adjusted by DT-ADJ potentiometer.
PWM / Dual	S1,S2 , S3	Operation mode can be selected by turning dead-time ON (PWM) or OFF (Dual).

Application Information

Typical Application Circuit

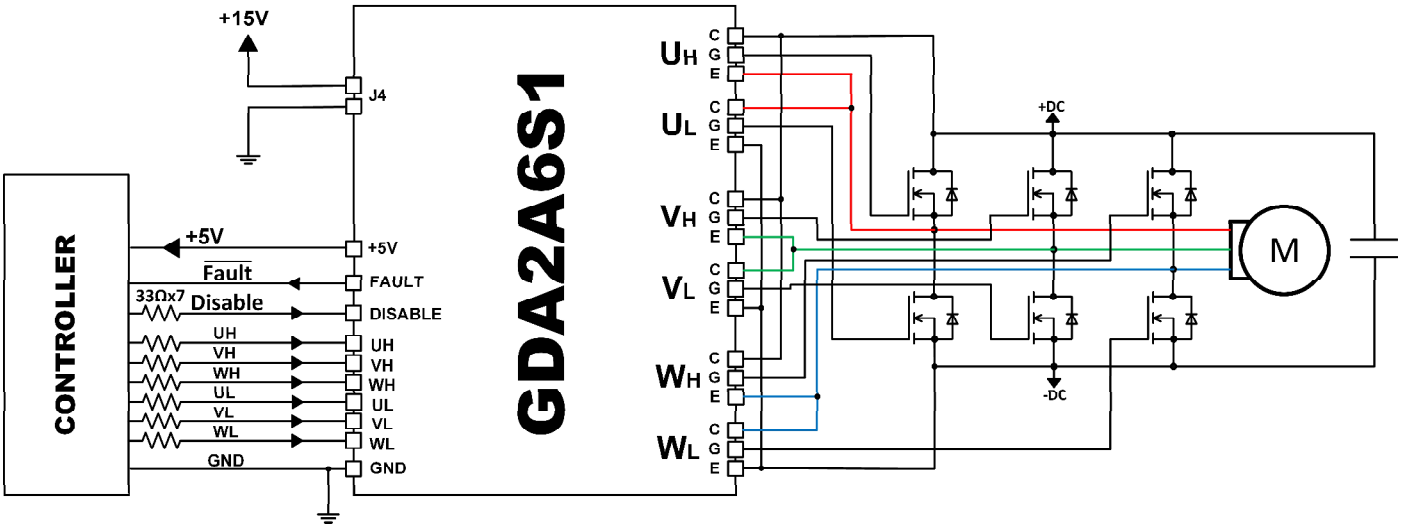


Figure 2: Typical application circuit

Operation Requirements

For proper operation of the gate drive module, certain requirements need to be fulfilled. First, the module need to be supplied with +15V voltage source through J4 or J1 connectors. Second, **all switches need be connected including collector terminals**, failure to do so will latch the fault circuitry and module will become un-operational. Last, control signals need to be given to the module with recommended 33 Ohm transmission resistors to avoid ringing and noise. Disable signal must be in low state, while Fault signal can be monitored for feedback.

Power Supply & Configuration (J2, J3& J4)

Supply voltage (+15V) is provided through J4 terminal block. It can also be supplied from J1 by connecting J2 jumper. Moreover, user can enable 5V output supply to external control circuitry by connecting J3 jumper.

Output Connection (J7-J18)

This module is designed to drive 3 phase inverter in half bridge configuration, the **lower switches share the same isolated source and hence low side drives (UL, VL & WL) cannot be used independently.** Output connectors from J7 to J18 should be directly connected to power switches accordingly. These connectors come in multiple options (free hanging, terminal blocks or headers for plug in module). Please note that voltage difference between the collector and rest of output is high, and hence proper wiring and insulation must be used. Gate and emitter wires are recommended to be in twisted pairs in case of free hanging connectors and must be as short as possible.

Fault Latch Disable (J6)

By default, fault latch logic is enabled to protect the switches from being damages, once a fault condition occurs, module will shut down and can only resume operation after power reset. However if the user wishes to control reset from the controller then J6 must be connected. At connected state, the fault latch will be disabled and module will resume operation after fault is cleared.

Fault output pin (J1.14) indicates fault condition at any switch and is active LOW. Once fault is detected, the output will be muted for 5µs (minimum). Any input

Application Information (Continued)

signal will be ignored during this mute period to allow driver to completely soft shut-down the IGBT.

Operation Modes (S1-S3)

User can select to use this gate driver as PWM or Dual input mode using 3 dip switches (S1-S3). All gate driver module are pre-configured in PWM mode by default. In PWM mode (S1-S3 ON State), UL, VL and WL signals are generated by dead-time generation logic. The user have to connect only UH, VH and WH signals to Input. In Dual mode (S1-S3 OFF State), all channels are independently controlled through respective signals, this is required for some topologies where shoot-through is needed such as Z-Source Inverter.

Configurable Dead Time (DT ADJ) in PWM Mode

User can configure the internal dead time using DT ADJ potentiometer. The duration of dead time delay DT can be calculated as per equation 1.

$$DT \approx 0.39579\ x\ RDT$$

Equation 1.

Where: DT= dead time (µs), and RDT= on board dead time programming trimmer (kΩ), which varies from 1k to 21kΩ, changing dead time from 0.39579µs to 8.3µs. By default, the module is configured at 2.2µs dead time.

Input & Output Indication LEDs, Test Points

LEDs are provided on input and output signals for instant user feedback. Input side LEDs are yellow colored. While output LEDs are independent for ON (Orange) state and OFF (Yellow) state so user can have feedback of high frequency PWM signals as well. Separate LEDs also indicate DISABLE (Orange), FAULT (RED) and Power state (Green).

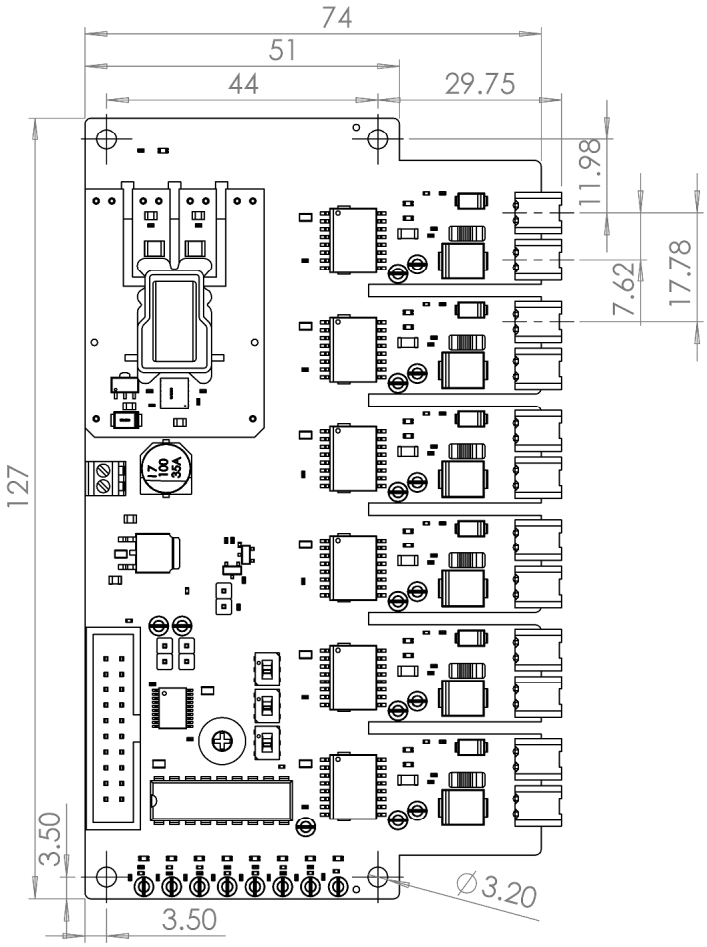
The module can also be supplied with input and output test points for easy debugging. This is very helpful feature for educational and research use. Test points are available on all inputs, Disable, Fault, Power (+15V, +5V, GND) and Gate, Emitter of all outputs.

Mounting and Safety

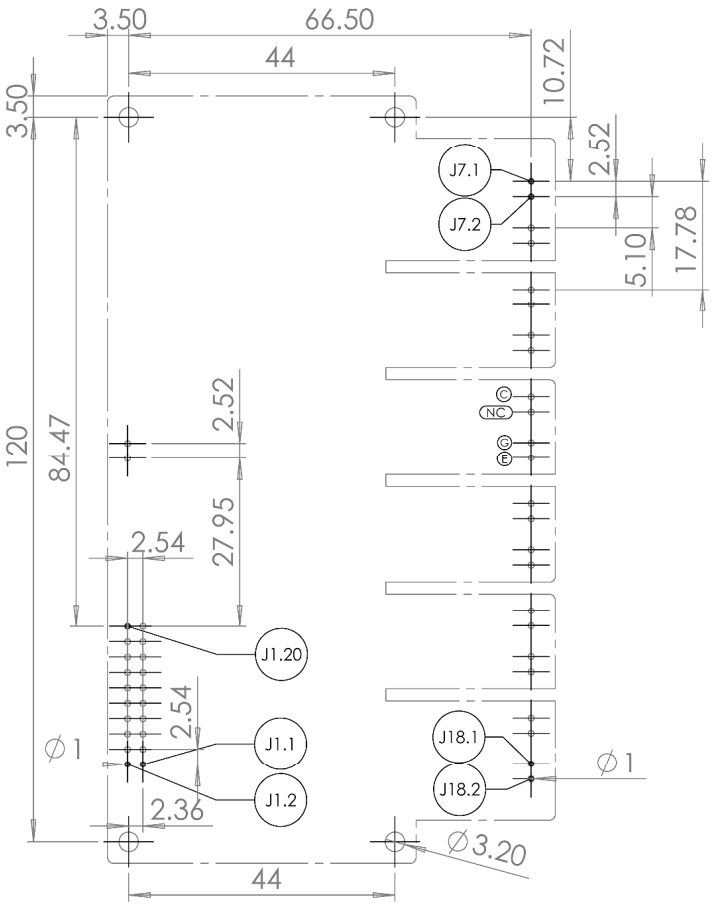
Since output side may carry dangerous high voltage, it is not safe to touch the circuit in operation. User must consider proper clearance of heat sink, metal enclosure, stray metallic objects near output side, and cover module and inverter with proper insulated casing. Care must be taken with mounting since mounting holes are close to outputs.

For more information, get our **Application Note** on how to design **Three Phase Inverter** to be used with our gate drive modules.
Visit: **www.taraztechnologies.com**

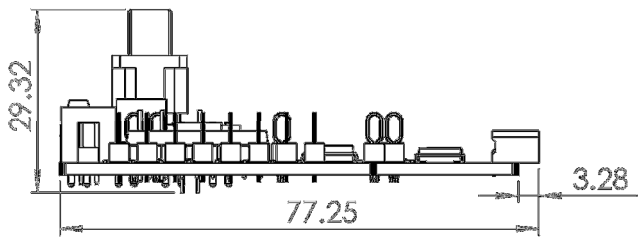
Mechanical Drawing



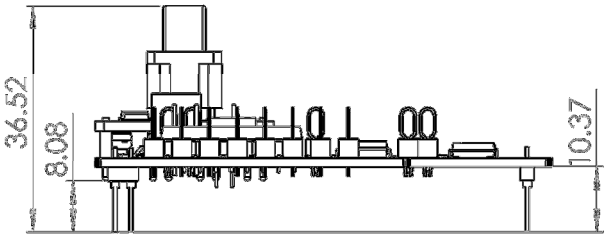
TOP VIEW



FOOTPRINT



SIDE VIEW (PX OPTION)



SIDE VIEW (PM OPTION)

Notes:

* All dimensions are in mm.

GDA-2A6S1

DATASHEET

Ordering Information

GDA - 2A 6 S 1 - XX - XX - XX/XX

- **GDA** - *Advanced*
- **GDS** - *Standard*

Gate Current *in Ampere*

Number of Switches

- **S** - *Single Supply*
- **D** - *Dual Supply*

Version

Operation Mode

- **HL** - *High/Low*
- **PW** - *PWM*
- **DL** - *DUAL*

Rg=

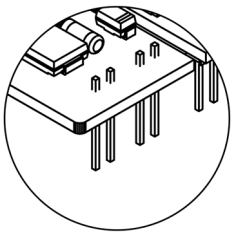
- *10Ω*
- *22Ω*
- *47Ω*

Options

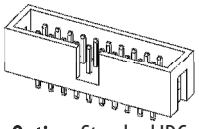
- **PM** - *Plug in Module, Bottom Side Headers*
- **PX** - *Pluggable Connectors*
- **TB** - *Terminal Blocks*
- **RA** - *Right Angle IDC* **(only with PX & TB)**
- **TP** - *Test Points*

Notes:

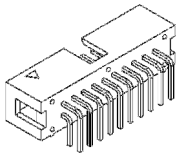
1) Either PM, PX or TB option can be selected.
2) Straight IDC is standard connector for J1 input connector and TB is standard for J4 connector. (Except in PM option)
3) PM (Plug in Module) option replace all connectors J1, J4 & J7-J18 with male headers soldered on the bottom side.
4) TP option can be selected with all configurations.
5) RA (Right Angle) option can be selected with PX & TB options only, which will replace standard straight IDC (J1) with right angle IDC.
6) The default gate resistor is 10Ω. However, user can control gate turn on and off speed by changing Rg to a lower value for faster switching or higher value to minimize ringing effect. The minimum value to be used should be greater than or equal to IGBT/MOSFET datasheet recommended value for reliable operation.



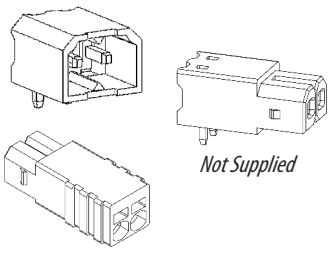
Option: PM
Plug in Module



Option: Standard IDC

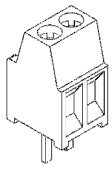


Option: RA-Right Angle IDC

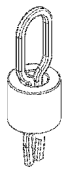


Not Supplied

Option: PX
1814841, 1704853, 1814980,



Option: TB
282834-2



Option: TP
Keystone THM MP

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